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PROOF-OF-CONCEPT EXPERIMENT REPORT

EVALUATION OF FABRICATION PROCESS FOR HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) BASED ON GaAs

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Proof-of-Concept experiment details

Main aim of the proposal: A new type of sensor element, similar to HEMT (high electron mobility transistor) with GaAs, based on 2.5-dimensional electron gas (between 2-D and 3-D electron gas), is starting to be investigated and first prototypes will be produced. Can this kind of architectures be achieved by the use of standard lithographic processes, such as the ones available in the region?

Because the electric fields in this device are weak, the device is very sensitive to external fields. The internal electric fields in this new type of HEMTs are at least an order of magnitude weaker in comparison to the fields in commercial HEMTs, and so it is more difficult than usual to achieve good ohmic contacts. The challenge is to fabricate suitable drain and source contacts for the device with lower electric fields.

Work plan:

1st step: Growth of MBE Layers

2nd step: Micro fabrication

3rd step: Characterisation after thermal treatment

Measurement author, dates and place: The MBE growth has been performed by dr. Giorgio Biasiol at Istituto Officina dei Materiali – CNR. The fabrication process and the characterisation after the thermal treatment has been performed by dr. Simone dal Zilio at Istituto Officina dei Materiali – CNR.

MBE layers growth

Epitaxial growth of the GaAs/AlGaAs semiconductor heterostructure was performed by solid-source MBE on a 2" (50.8mm) semi-insulating GaAs (100) wafer, 350 um thick. Growth rates were calibrated before the actual sample was grown on a test substrate by optical reflectometry, ensuring a precision better than 1% in layer thickness and composition. Silicon was used for n-type doping; doping calibration is done periodically through Hall effect measurements at different Si fluxes. The heterostructure layer sequence was as follows:

- + First layer: GaAs
- + Second layer: $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$
- + Third layer: GaAs
- + Fourth layer: n-GaAs

Fabrication design

We design a suitable fabrication workflow following the requirements of the company. The design of the mask has been accomplished, producing the CAD file containing the elaborated 4 masks.

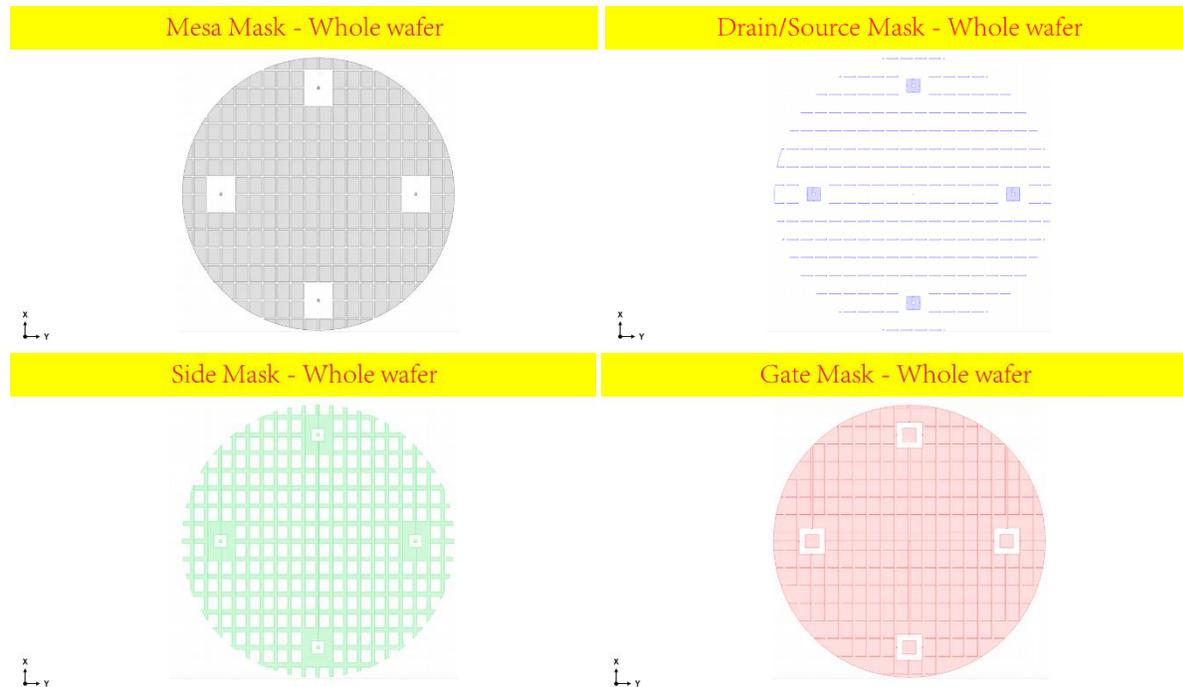


Figure 1 UV lithography masks CAD

Microfabrication

In the following, the fabrication protocol employed for the production of the test wafer is described.

Fabrication of MESA

- Cleaning of the wafer in acetone for 5 sec and subsequent drying by N2 blowing.
- Oxygen plasma cleaning: 20W, BIAS 40V, Time 1 min
- Resist Deposition: S1813 3500 rpm, bake 115°C 1'
- Exposure with Mask 1 – MESA
- Develop I MF319, 20°C 45", rinse with H2O
- Wet Etching in H3PO4:H2O2:H2O (1:2:50) 3' 15 sec
- Resist stripping by hot acetone

GATE Deposition

Mask 2 - GATE

- Resist Deposition: S1813 3500 rpm, bake 115°C 1'
- Exposure with Mask 2
- Develop I MF319, 20°C 45", rinse with H2O

Metal Deposition – GATE contacts (Cr, Au)

- Deposit 10 nm of Chromium (Cr)
- Deposit 80 nm of Gold (Au)

Lift-off

Remove photoresist and metal on top of the photoresist by acetone

DRAIN & SOURCE Etching

Oxygen plasma cleaning

- Resist Deposition: S1813 3500 rpm, bake 115°C 1'
- Exposure with Mask 3
- Develop I MF319, 20°C 45", rinse with H₂O
- Wet Etching in H₃PO₄:H₂O₂:H₂O (1:2:50) 3' 15 sec
- Resist stripping by hot acetone

Measure thickness and check surface roughness with profilometer.

STENCIL Mask Preparation

Start from SiN coated (2000 nm) Silicon wafer.

- Cleaning in Oxygen plasma
- Deposition of Cr thin film (150 nm) by DC magnetron sputtering
- Resist Deposition: S1813 3500 rpm, bake 115°C 1'
 - Exposure with Mask 4
 - Develop I MF319, 20°C 45", rinse with H₂O
- Wet etching of Cr layer
- Dry etching in RIE of SiN
- Wet etching in KOH 30%, 90°C
- Removal of Cr and SiN from the surface

Deposition of DRAIN & SOURCE trough STENCIL

- Alignment of Si STENCIL mask: Check the alignment under the microscope
- Transfer into the evaporator
- Deposition DRAIN & SOURCE Contacts (Ge-Au, Ni, Au)
 - Deposit 40 nm of germanium-gold (Ge-Au)
 - Deposit 7 nm of nickel (Ni)
 - Deposit 53 nm of gold (Au)
- Lift off in hot acetone

Characterization of the fabricated sample

One of the main requirements was the perfect alignment of the drain and source electrodes with the etched structures. The alignment through consecutive lithographs was evaluated as not sufficient, for the current state of the instrumentation used. For this reason, an alternative process has been proposed based on the use of the same resist masking to carry out the wet etching process first and then the

deposition and lift off process of the metal electrodes (see the following image for the schematic description of the process).

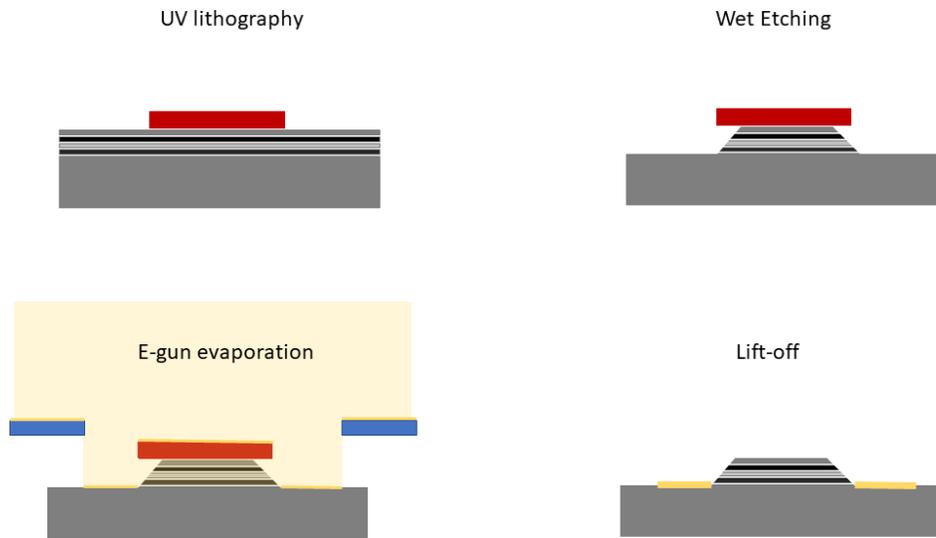


Figure 2 Process scheme for the deposition of source and drain electrodes

The characterization of the test samples produced was carried out by means of SEM at the IOM-CNR laboratory. In the following images it is possible to verify that the strategy of using the stencil mask for the deposition of drain and source allows an excellent alignment. The problem highlighted is that of having a better alignment system between stencil and sample, in terms of positioning and stability for transfer to the deposition chamber. For this purpose, a system dedicated to the purpose will be developed in agreement with the company, which can be adapted to the instrumentation present in the IOM-CNR laboratory (inverted optical microscope and e-gun evaporator).

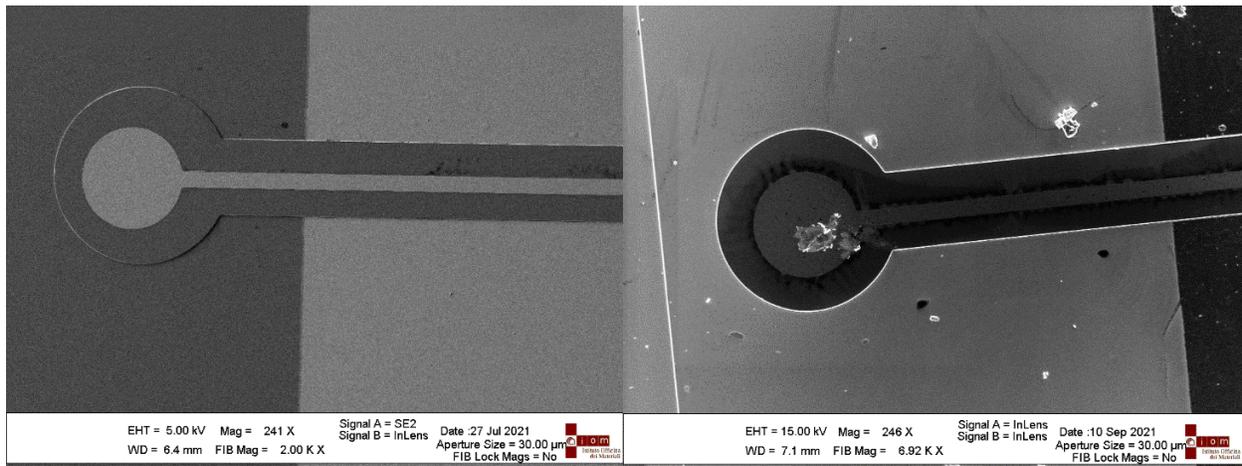


Figure 3 SEM images showing the alignment of the drain and source electrodes with the etched structures.

Characterization of the samples after thermal annealing.

The samples were characterized after the thermal treatment (annealing) in order to verify the reason of the degradation of the electrodes after the process

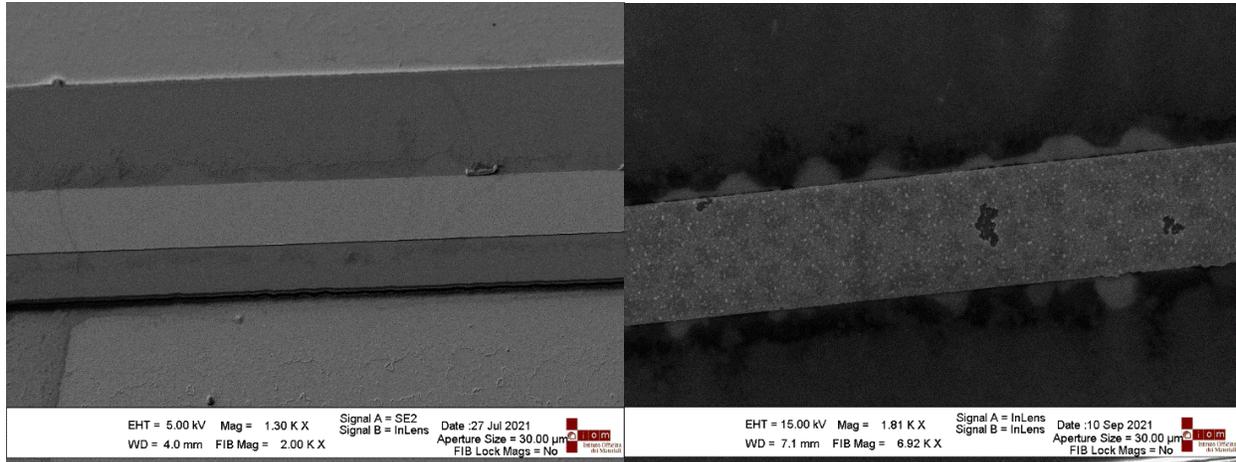


Figure 4 Detail of the evaporated electrodes before and after the annealing treatment.

The formation of nanoclusters on the metal electrodes can be related to the presence of organic contaminations. The brighter structures around the electrodes can also indicate residuals of resist or solvent after the stripping procedure.

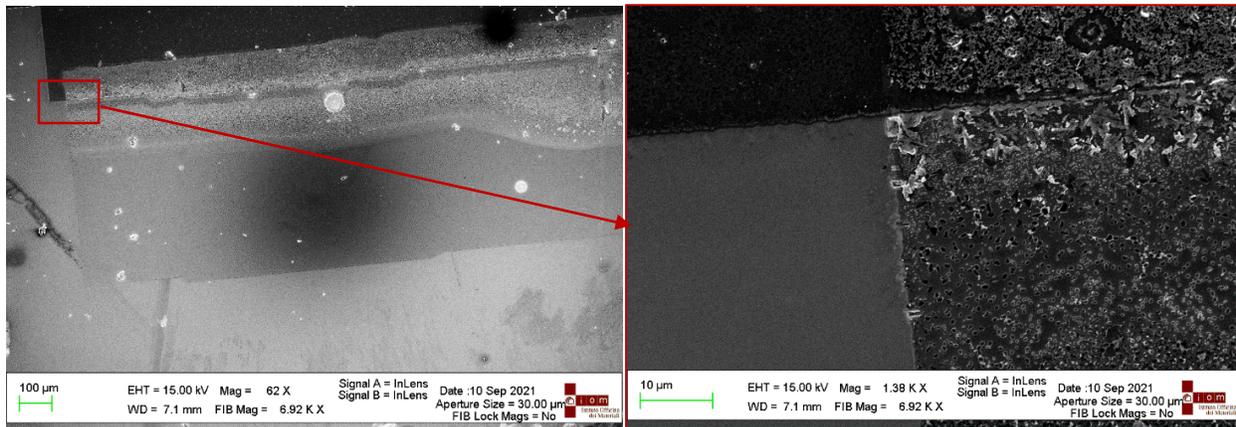


Figure 5 First and second evaporated electrodes.

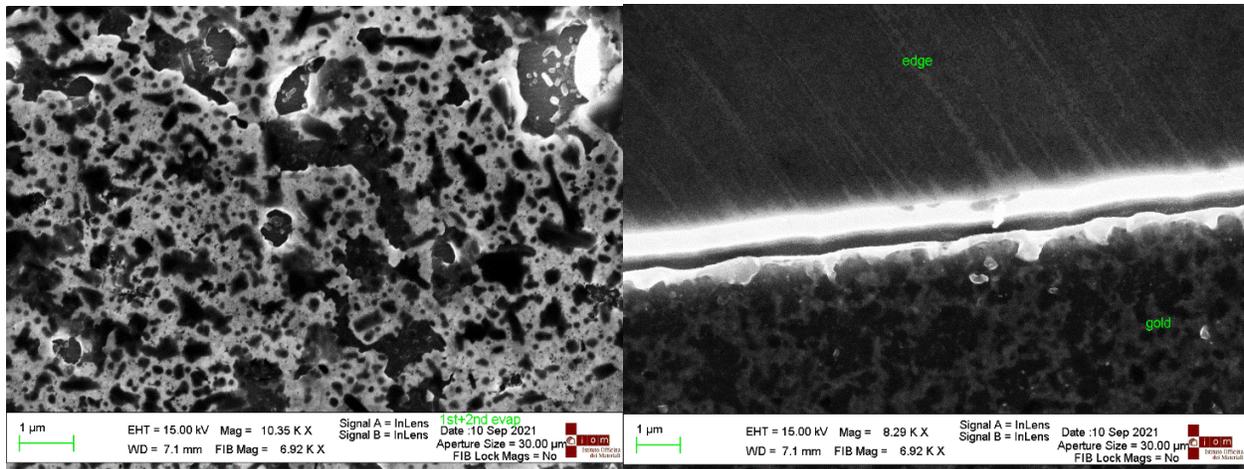


Figure 6 Details of the metal electrodes multilayer after thermal annealing

It seems that one of the problems is the poor adhesion of the metal thin film on the substrate. The darker spots could be related to the presence of carbon contaminations adsorbed during the alignment procedures. A controlled oxyplasma treatment after the alignment could solve the problem. In any case, a faster procedure during for the alignment seems to be strongly recommended. The poor adhesion is also confirmed by the cross sectioning in the following image where the presence of a gap between the substrate and the thin metal film is highlighted.

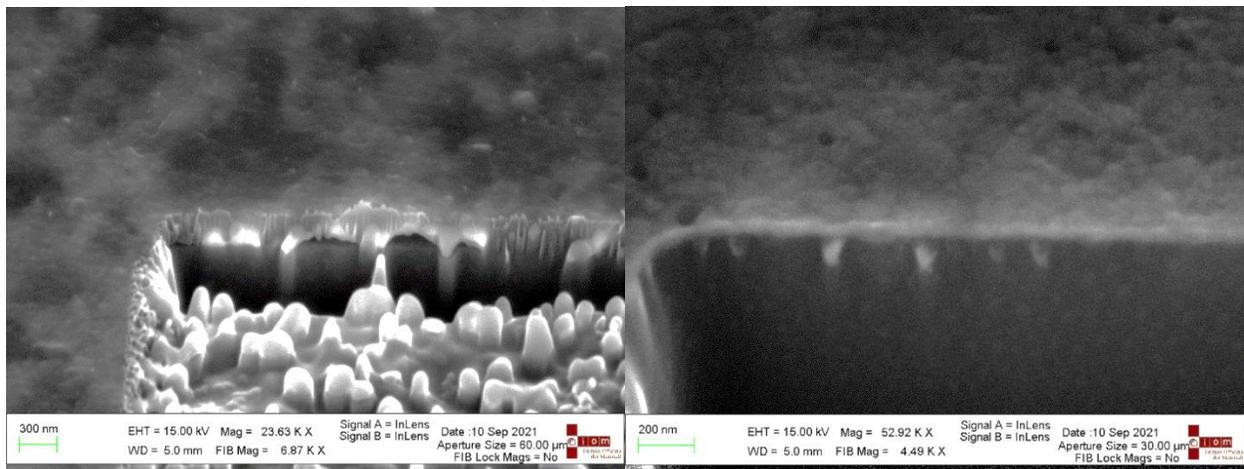


Figure 7 First and second evaporation detail after FIB cross sectioning

The first evaporation looks to be better in terms of adhesion, as visible in the second cross sectioning image. After the annealing treatment the interface between metal and substrate is less visible, indicating the diffusion has occurred.

Conclusion

For the fabrication of the devices, a process scheme based on a series of aligned lithographs, wet etching processes and controlled depositions of metallic films was developed. The proposed process scheme was tested on a wafer suitably grown by MBE. From the characterizations carried out on the devices made by the company and IOM-CNR, it is clear that the process scheme is effective, but the manufacturing strategies must be further implemented in order to avoid mainly surface contamination that can affect the final result, especially in terms of quality in the metal films and in its adhesion / contact. It is proposed to introduce further intermediate cleaning steps, based on wet and plasma processes. Furthermore, it is suggested to develop a suitable alignment system for positioning the stencil mask for the final deposition of the electrodes.

This report has been written by Simone dal Zilio on 05/11/2021