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PROOF-OF-CONCEPT EXPERIMENT REPORT

CROSS-SECTION ANALYSIS OF AN INTEGRATED CIRCUIT

Authors:

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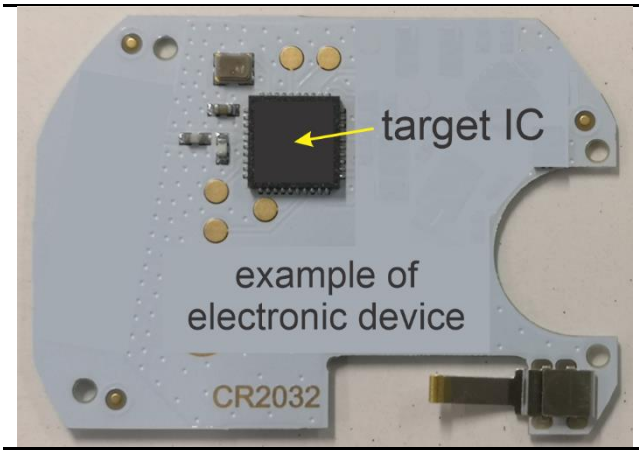
Proof-of-Concept experiment details

Received sample: the company provided several samples of functional electronic device where IC components are presents, attached to a flexible plastic support i.e. printed circuit board (PCB).

Fig. 1: Samples delivered by the company



Samples:
several functional electronic devices (same type – V12) with IC components attached to PCB (Target IC visible on image)

Delivery date: March 7th 2021

Planned analysis:

1st Binocular microscope inspection of delivered electronic devices, followed by SEM-EDX preliminary analysis of a metallographic polished PCB at a cross-section with target IC component. The preliminary analysis was aimed to evaluate IC component attachment with PCB and to obtain detailed insight of the target IC internal structure.

2nd Preparation of a large cross-section by Ar^+ ion polisher at 2 selected positions of the target IC component

3rd SEM/EDX analysis of the resulting Ar^+ ion polished cross-sections

4th Optional: FIB-SEM cross-sectional analysis if Ar^+ polisher technique will not provide sufficient results.

Sample preparation:

Metallographic specimen preparation: the electronic device was parallelly cropped out on both sides so that the target IC device could be perpendicularly aligned into metallographic mold (ϕ = 3 cm), embedded with general purpose epoxy resin (KEP Epoxy, Kemet, UK) and cured for 10h at room temperature. Embedded specimen was grinded with water lubricated abrasive, in sequence by using progressively finer abrasive grits, until smooth cross-sectional surface was exposed at the middle of target IC component. In a final stage, specimen was polished with diamond paste to a mirror finish, cleaned with ultrasound in distilled water/ethanol and dried in vacuum overnight. Prior SEM investigation metallographic sample was coated with amorphous carbon (8 nm) by sputter coating system (PECS, Gatan, US)

Ar^+ X-section polishing: the device parts out of the IC were cropped out. The plastic support below the IC has been left attached below the IC. The IC has been glued with resin directly on the cross-section polisher mount. After the polishing (before SEM/EDX analysis), the X-section has been coated with amorphous C (6 nm) by sputter coating system (PECS, Gatan, US).

Measurement author, dates and place:

Metallographic specimen preparation of the electronic device followed by preliminary SEM-EDX analysis was performed by Gregor Kapun in time period from 11/05/2021 to 07/06/2021 at CENN - Nanocenter, Jamova cesta 39, SI-1000 Ljubljana, Slovenia

Large Area Mapping of mechanically polished IC component has been performed by Gregor Kapun at National Institute of Chemistry, Hajdrihova 19, SI-1000 Ljubljana, Slovenia

Ar^+ ion cross-section polishing has been performed by Andraž Mavrič and Mattia Fanetti at University of Nova Gorica, Vipavska 11c, 5270 Ajdovščina, Slovenia

SEM/EDX analysis of initial Ar^+ ion polished IC sample was performed by Gregor Kapun on 05/07/2021 at CENN - Nanocenter, Jamova cesta 39, SI-1000 Ljubljana, Slovenia

SEM/EDX analysis of the Ar^+ ion polished samples were performed by Andraž Mavrič and Mattia Fanetti in time period from 18/06/2021 to 18/08/2021 at University of Nova Gorica, Vipavska 11c, 5270 Ajdovščina, Slovenia.

Preliminary measures:

Initial sample observations were done with binocular stereo microscope followed by SEM-EDX analysis of metallographic polished cross-sectional area of the electronic device at the target IC component. In addition, Large Area SEM-BSE image as well as Large Area EDX Mapping were acquired across polished cross-sectional area to obtain general insight into internal structure of the IC component and its integration to PCB support.

Observation/processing conditions:

SEM/EDX analysis at CENN: performed by UHR-SEM Verios G4 HP (Thermo Fisher, The Netherlands), equipped with SDD Ultim Max 65 EDX detector (Oxford, UK). Software for EDX analysis AZtec 4.3 (Oxford, UK). Beam energy 5-15 keV; secondary electron detector, backscattered electron detector.

Large Area EDX Mapping at NIC: performed by FEG-SEM Supra 35 VP (Zeiss, Germany), equipped with SDD Ultim Max 100 EDX detector (Oxford, UK). Software AZtec 5.0 + LAM automation (Oxford, UK). Beam energy, 20 keV, beam current 1.2 nA, secondary electron detector, backscattered electron detector. LAM was obtained with fully automated acquisition of 330 individual map sub-regions, followed by their montage into a single area TrueMap data with final resolution of 13.158 x 4.802 px.

Ar^+ cross-section polishing: performed by JEOL IB-09010CP, Ar^+ ion energy 5.5 KV; current: 140 mA; polishing time 4.5 hr. Stage swinging during polishing.

SEM/EDX analysis at UNG: performed by FEG-SEM JEOL JSM 7100f equipped with Oxford X-Max 80 EDX detector. Software for analysis: AZtec 4 (Oxford, UK). Beam energy 5-15 KeV; secondary electron detector, backscattered electron detector.

Main aim:

The main aim of the POC experiment is to analyze the internal structure of an integrated circuit (IC). In particular, to verify if Ar^+-ion polishing is effective for the preparation of X-sections of ICs and if SEM/EDX is appropriate to analyze the X-section (and to which resolution).

Findings of the preliminary analysis

1. SEM/EDX analysis of mechanically polished specimen

Prior preliminary analysis, metallographically polished cross-section was generated throughout the entire electronic device with an imaging plane set at the middle of the target integrated circuit (IC) component as shown in Figure 1a. Therefore, the obtained cross-sectional area included both, target IC component and printed circuit board (PCB) support as presented in top-down optical image (Figure 1b). Large area SEM-BSE image (Z-contrast) of the target cross-sectional area (Figure 1c) reveals that IC is enclosed within insulating case with dimensions of 4.68 mm x 0.95 mm (width x height) and attached to a PCB support. Even more detailed insight, with chemical identification of each individual component, can be revealed from Large Area EDX Mapping (LAM) which is presented as EDX Layered image and individual element maps in Figure 2. In the bottom-up order, the PCB support consists of laminated sandwich structure of copper (conductive) and titanium oxide (insulator) supported by brominated polymer matrix (non-flammable) which is reinforced by fiber glass bundles (Ca, Al, Si, O) in its middle section. Copper pads on top of PCB were found Nickel-Phosphorus plated, which is commonly used in PCB designs to prevent copper corrosion and ensures good intermetallic connection between contact pad and IC during soldering process. Nanostructured IC layer (target/aim of the planned analysis) was identified on top of Si wafer (positioned in the middle of encapsulated IC component), which appears to be glued with a conductive (electron and thermal) silver adhesive to a thick copper contact. The later was found directly contacted via tin soldering to one of the PCB contact pads. It is also evident that target nanostructured IC layer is buried 350 μm below insulating case and it is present across whole Si wafer length (2.40 mm). Within insulating case also some copper spots are seen, which are actually cross-sectional projections of numerous copper wires, which connects various functional sites of nanostructured IC layer (in top-down direction) to the outside contacts that are soldered to the PCB.

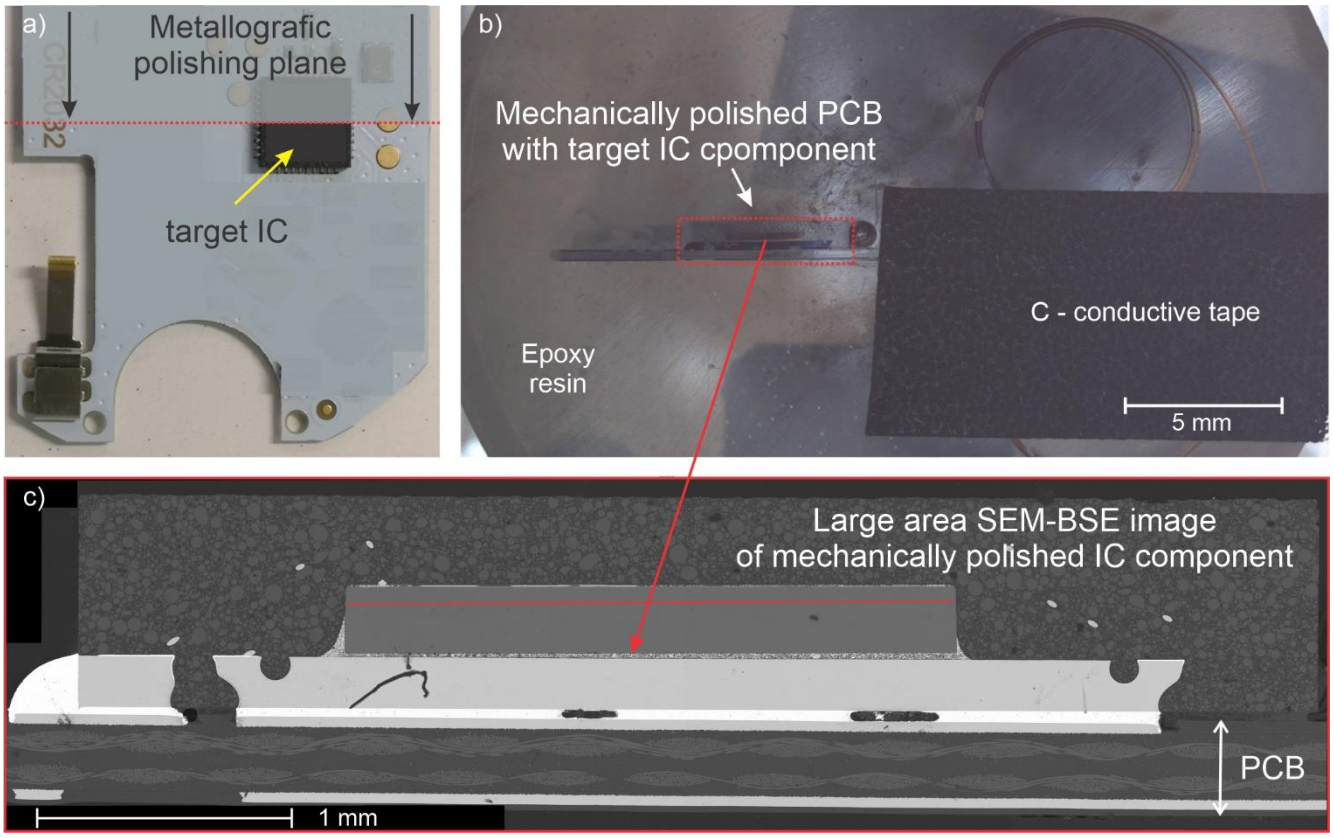


Figure 1: Position of mechanically polished electronic device (a) with optical image of freshly exposed cross-section - target IC component on top of PCB (b) and corresponding large area SEM-BSE image (c)

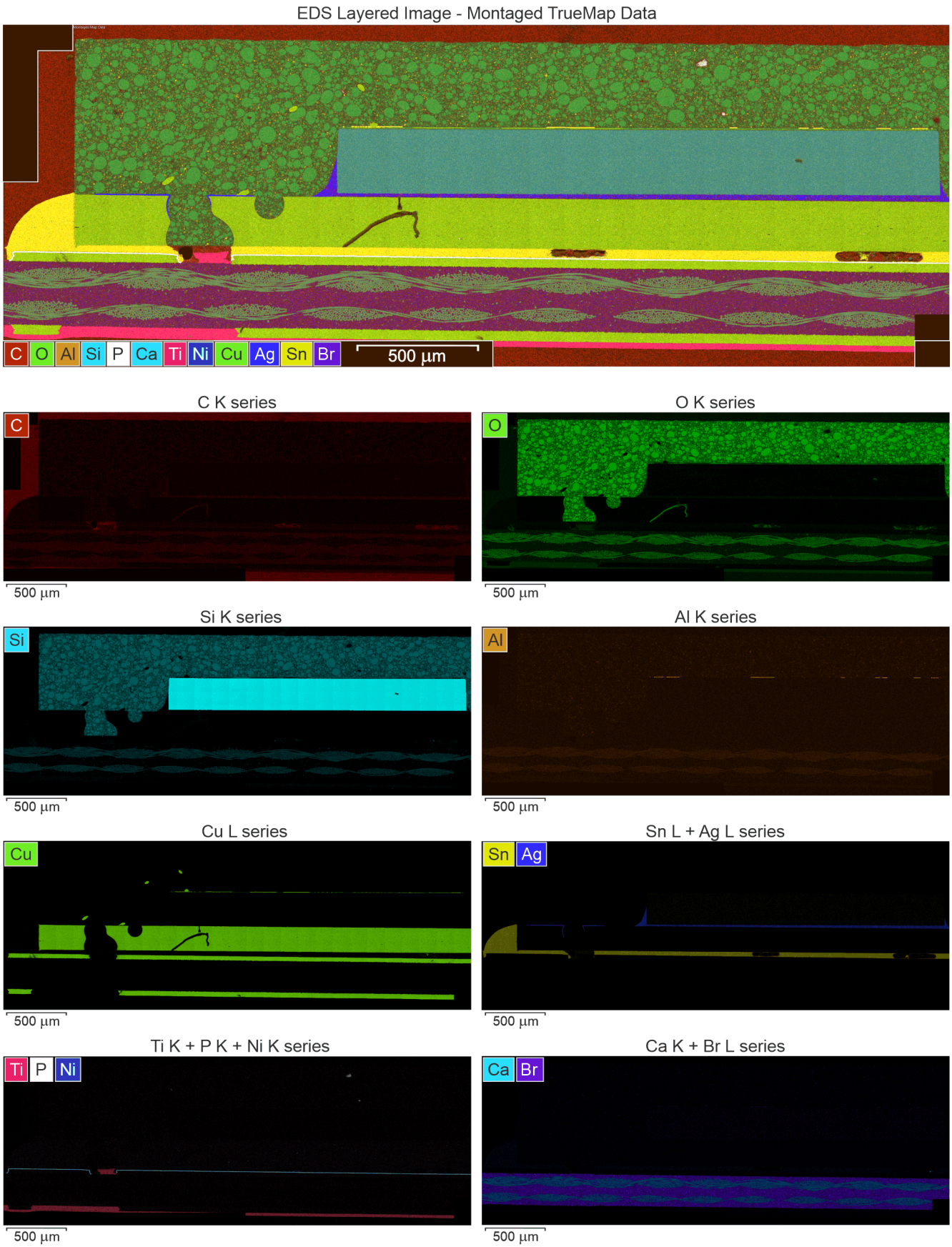


Figure 2: Large Area EDX Mapping (montaged from 330 individual map sub-regions) of polished IC component ontop PCB, which is presented as EDX TrueMap Layered image and corresponding individual element maps

First impression and some general overview of IC nanostructured layer can be obtained from phase contrast SEM imaging of the metallographically polished specimen. Figure 3a-3b shows SEM-BSE images of top-left and top-right edge of Si wafer with highlighted nanostructured IC layer. Example of copper wire contacting the functional IC site can be seen at the enlarged image of the left edge (Figure 3c). However metallographic polishing approach turns out as inappropriate way of IC sample preparation for detailed SEM analysis. This is evident form higher magnification SEM image shown in Figure 3d, where mechanical damage and contamination of cross-sectional surface, caused by mechanical polishing, significantly limits insight into nanostructure IC layer components. To overcome this problem, intrinsic (damage and contamination free) cross-sections must be prepared by using advanced sample preparation techniques such as Ar^+ ion polishing of FIB milling.

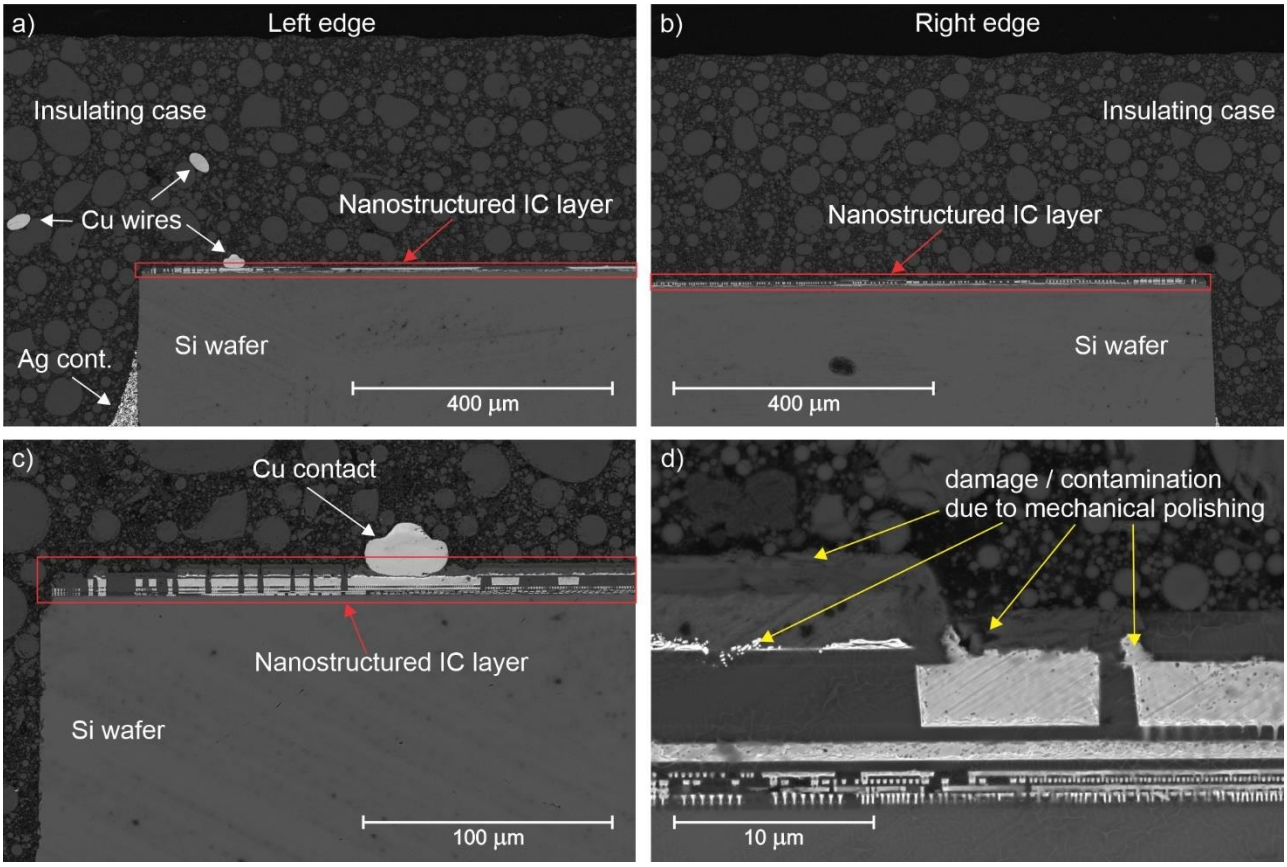


Figure 3: Phase contrast SEM images of mechanically polished IC component cross-section

Results

1. Cross-section polishing by Ar^+ ions

The Ar^+ ion cross-sectional polishing has been performed in two different positions (Pos.1 and Pos.2) on the IC as denoted with red and yellow lines in Figure 4.

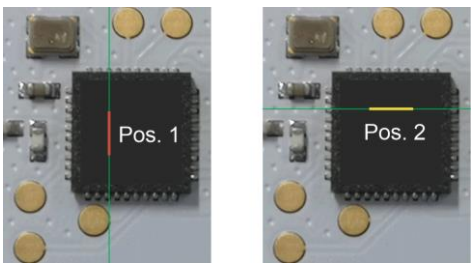


Figure 4: Locations of Ar^+ ion polished cross sections on the IC

In both polishing processes, the result is a successfully polished region with a top width of about 1.5 mm and a depth of 650-700 μm. The width of the polished »active« layer (on top of the Si substrate) is roughly 900 μm.

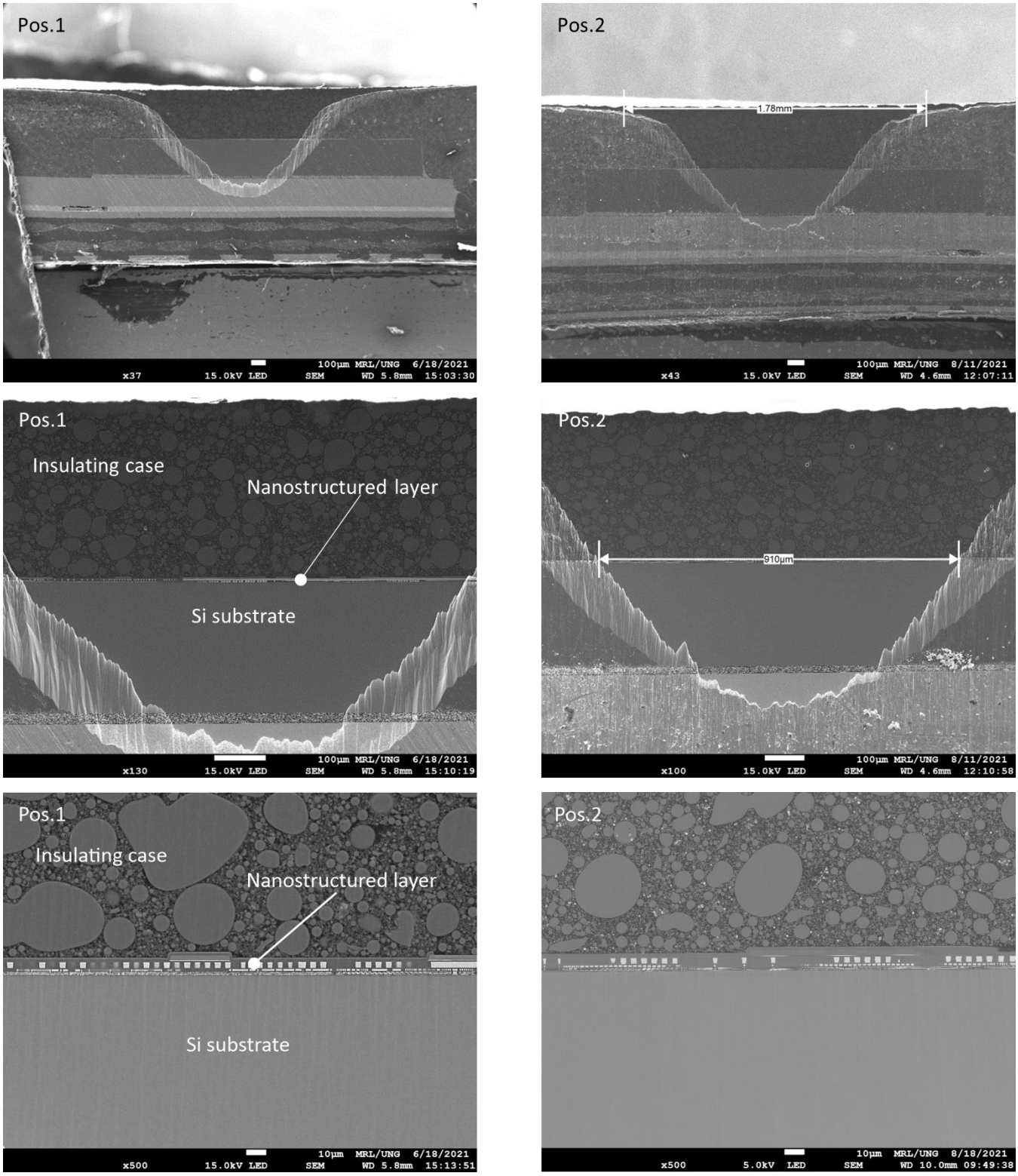


Figure 5: Low-mag SEM images of Ar^+ ion polished cross sections at positions 1 and 2

2. SEM analysis of Ar^+ ion polished IC cross sections

High magnification SEM allows for clear observation of the elements in the nanostructured layer. Some images are following in Figure 6.

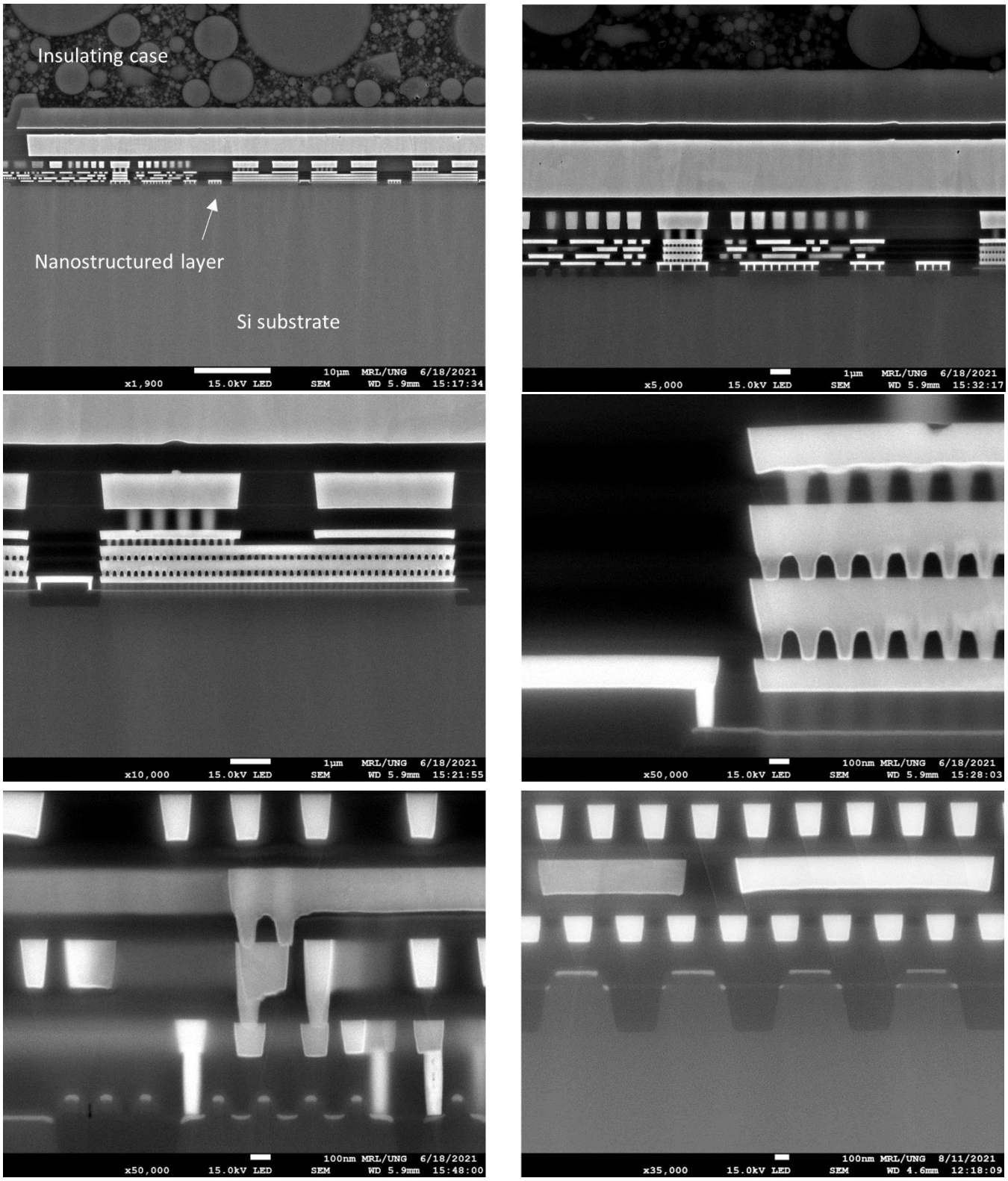


Figure 6: High magnification SEM images of Ar^+ ion polished cross sections of nanostructured IC layer

As evident form Figure 7, the features sharply visualized (some indicated in blue) are at the X-section surface, while the broad features (some indicated in red) are beyond the surface.

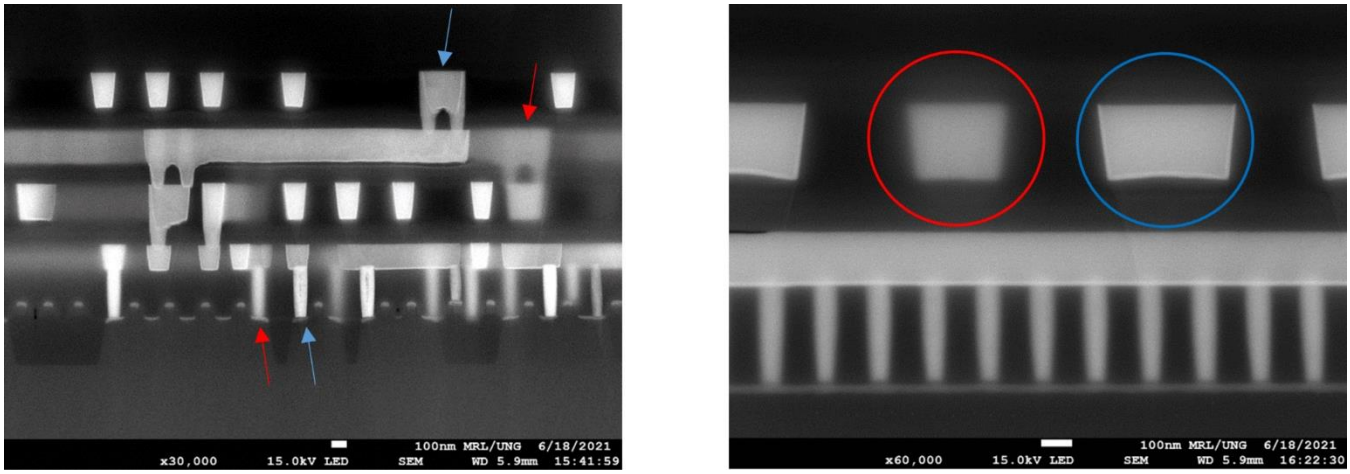


Figure 7: SEM images with highlighted features at the X-section plane and beyond the surface

The almost complete absence of surface morphology features, due to the flatness of the X-section, makes the observation with secondaries almost equivalent to the one with back-scattered, potentially with some higher resolution. However, especially at high magnification, the observation with backscattered electrons allows for higher elemental contrast (with heavier elements brighter). Some examples are shown in Figure 8.

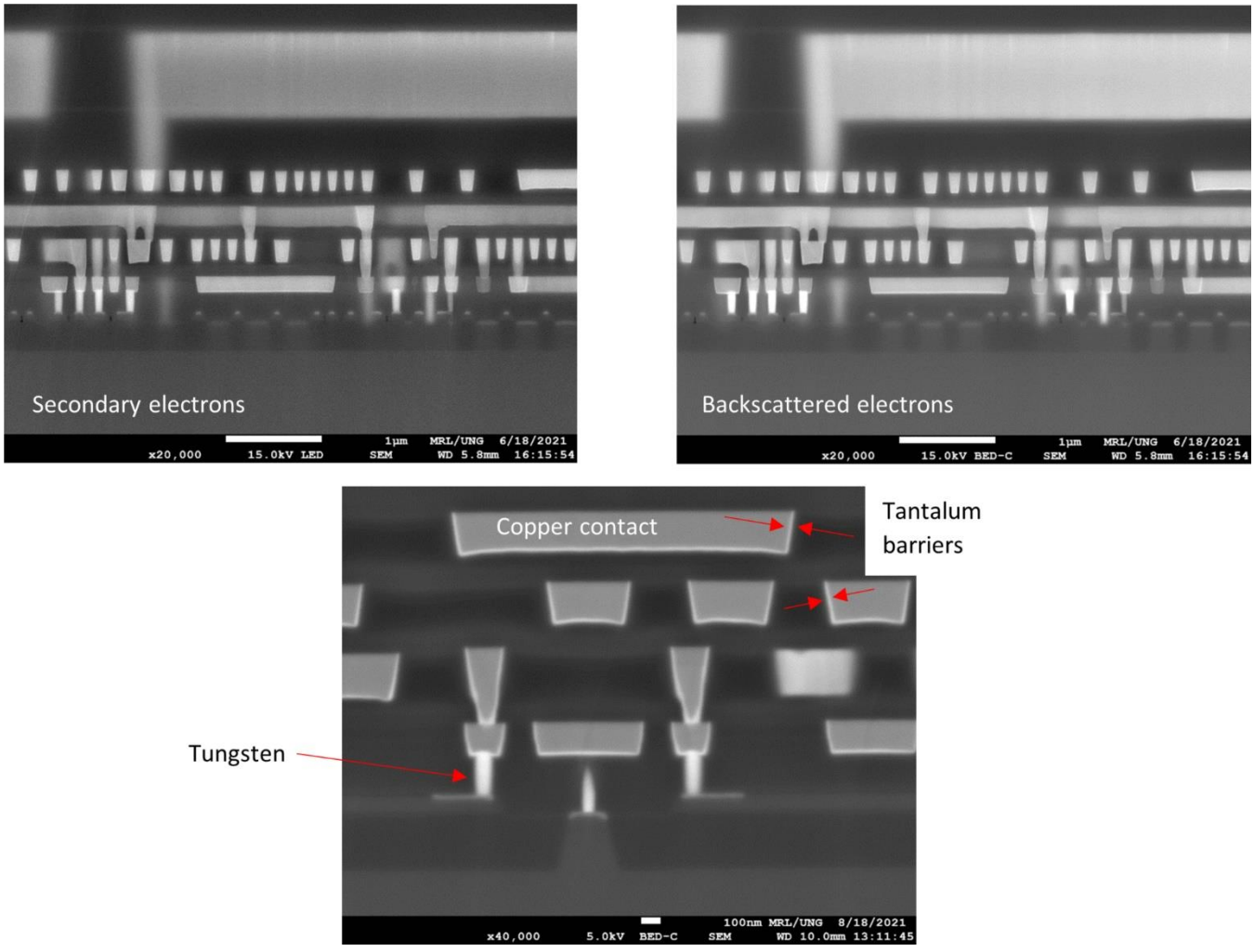


Figure 8: High magnification SEM images of Ar^+ ion polished cross sections of nanostructured IC layer

3. EDX analysis of Ar^+ ion polished IC cross sections

EDX analysis on the X-section allows for the recognition of the elements in each feature. The elements found in the nanostructured layer are: Si, O, N (in the substrate - N is present at the doped and dielectric layers); Al, Cu (in the contacts) and Ta, W, Ni (in the barriers and in other small features). A typical set of EDX maps for major elements is shown in Figure 9, together with the electron image.

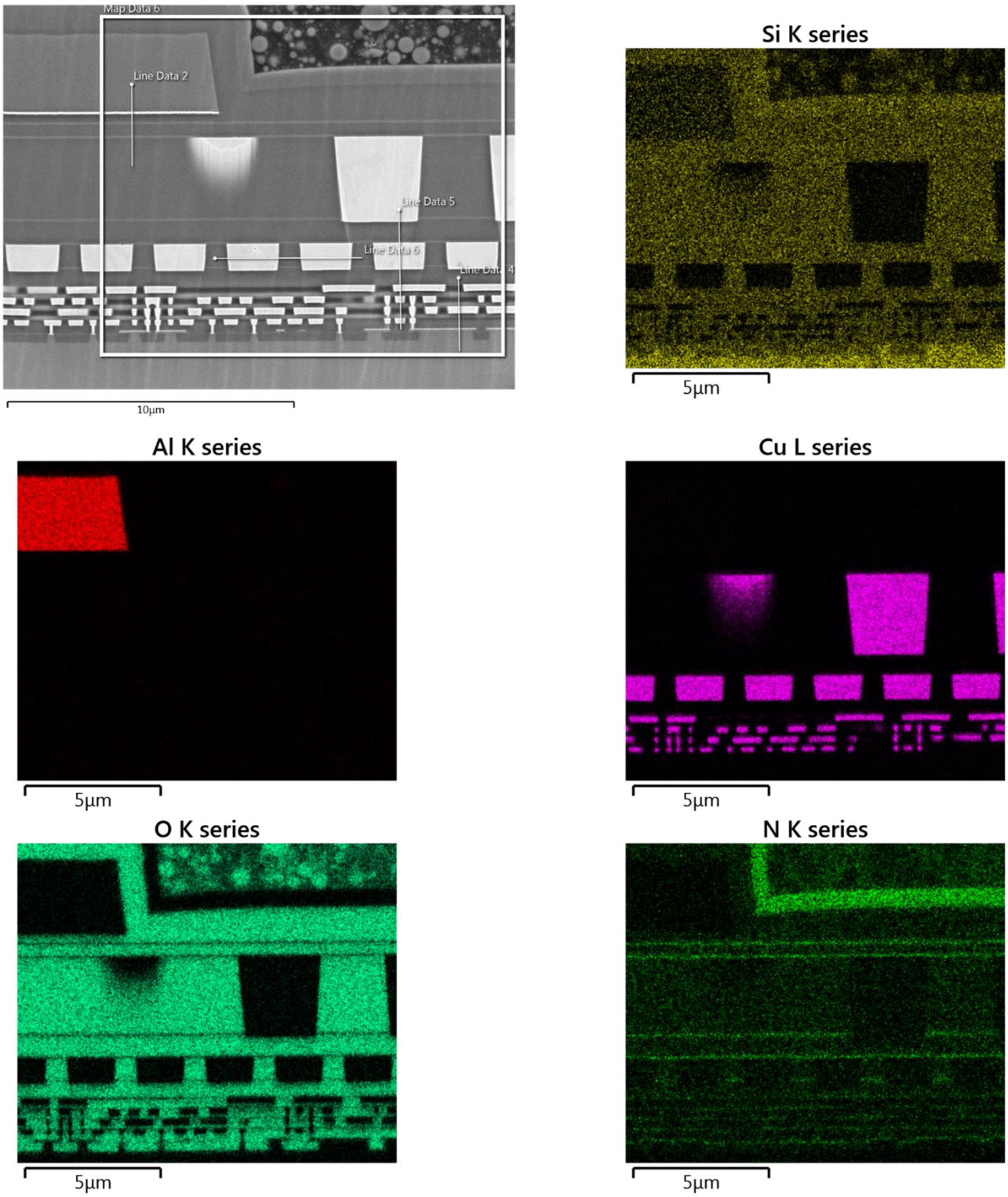


Figure 9: Typical set of EDX maps for major elements in nanostructured IC layer

For minor components (W, Ni, Ta) in several cases an overlapping problem occurs, for example W M line (1.774 KeV) and Ta M line (1.842 KeV) overlap with Si K line (1.739 KeV) and Ni L line (0.851 KeV) overlaps with the satellite of Cu L line. To avoid the issue, one can decide to map the high energy lines, such as Ni K, W L and Ta L. However, high energy lines give often low signal and poorer lateral resolution. Another option is to use low beam energy (e.g. 5 KeV) and use the low energy lines. In this case, point-by-point deconvolution of the EDX map is necessary, to overcome the overlapping problems. In most cases, by means of deconvolution routines, it is possible to effectively separate the contribution of different elements and obtain the correct maps. As an example, minor elements maps are shown in Figure 10, acquired at low beam energy (5 KeV) and after software deconvolution.

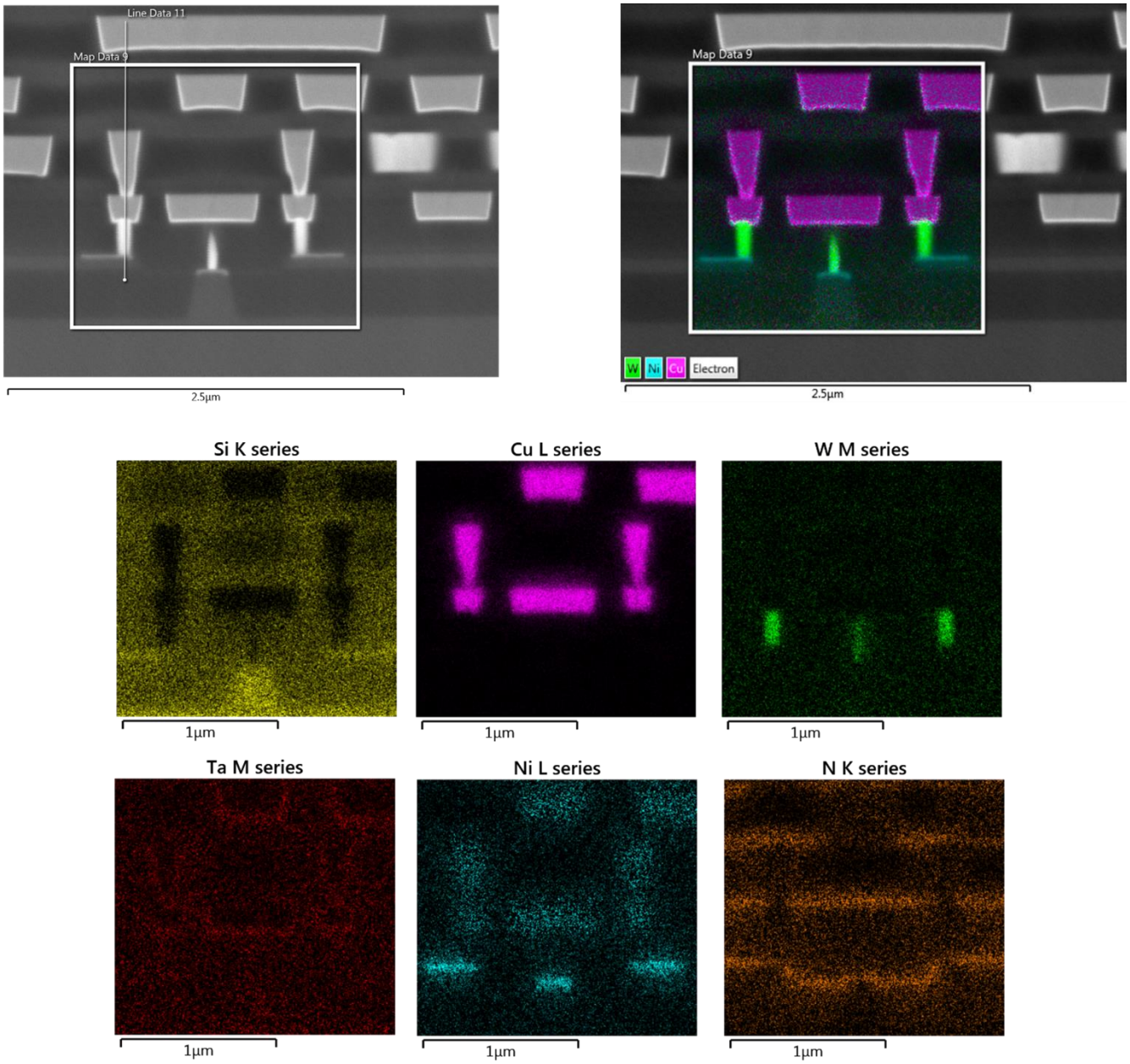


Figure 10: EDX elemental mapping at 5 KeV after point-by-point deconvolution of the EDX data

In some cases, a line profile is a better choice to identify different materials in a shorter time. In the following a line profile is shown. Again, using low beam energy (5 KeV) allows for higher lateral resolution. Also in this case, a deconvolution routine is necessary to avoid wrong profiles due to line overlap.

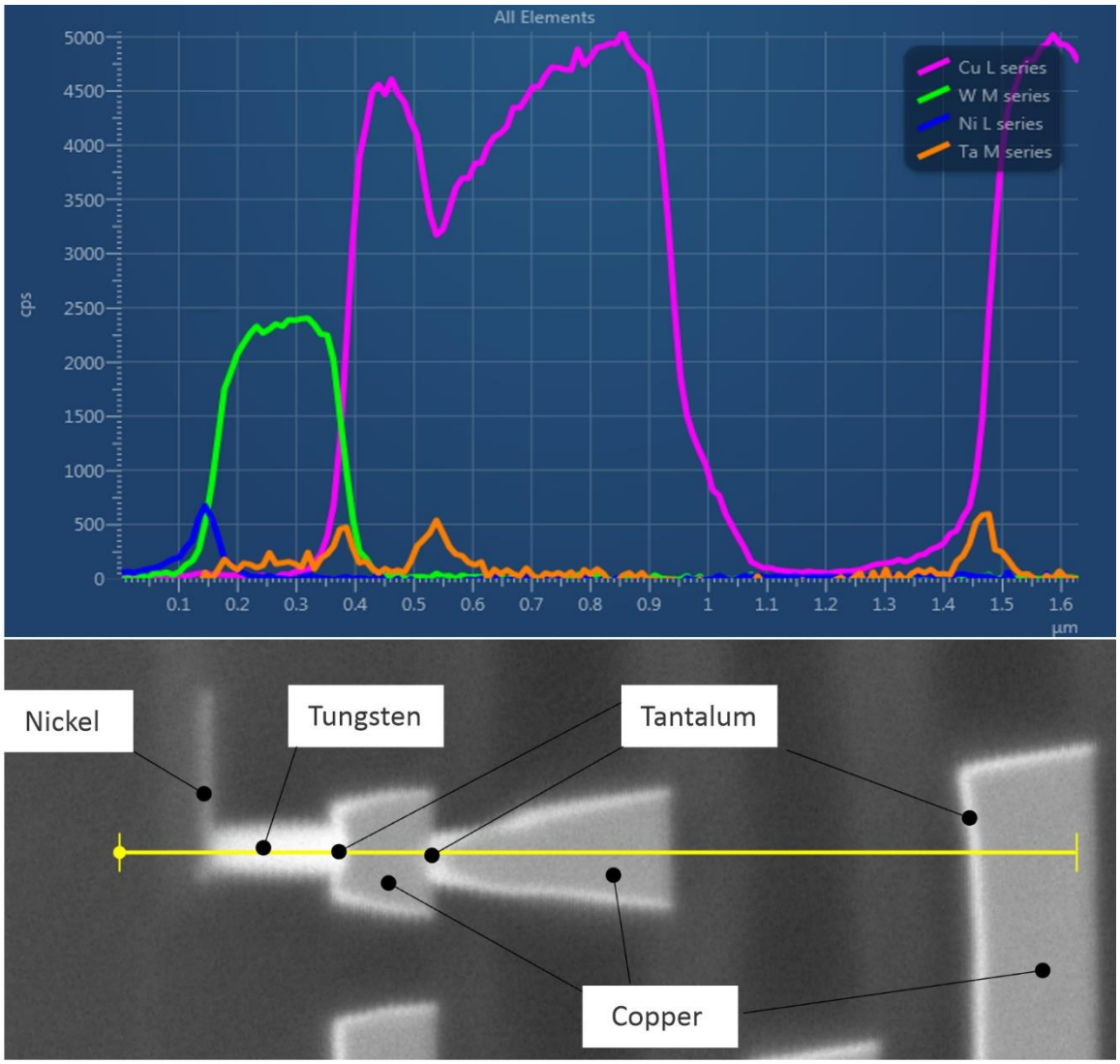


Figure 11: EDX Linescan profiling at 5 KeV after deconvolution of the EDX data

Concluding remarks on the capabilities of the demonstrated techniques

By Ar^+ ion milling it is possible to easily obtain a large X-section of an IC without additional steps. Before observation, a coating with C is performed, to make the sample conductive. The X-section is smooth enough to resolve all the features by SEM without problems, down to the resolution limit of SEM (few nm). The main shortcoming in the use or Ar^+ ion milling is the poor capability in localizing the cut. The accuracy in the positioning of the shield for cutting is approximately 50 μm.

The use of focused Ion Beam FIB would in principle allow for a much higher accuracy in the X-section localization but presents two major drawbacks: 1) it is not possible to cut through the insulating case, which is about 400 μm thick. Hence, it would be necessary to remove the insulating case before the X-sectioning. 2) the generated area of the X-section would be smaller (in the case of Ga-FIB typically limited to 80 μm in width and 40 μm in depth).

Once the X-section is produced, EDX analysis allows to identify the main composition of the features, included small features. The use of low beam energy (5 KeV or less) allows for good lateral resolution in the maps, with possibility in some cases to resolve details <100 nm (e.g. Ni layers <50 nm). However, at low beam energy the overlapping between emission lines becomes a frequent issue, and an effective software (like the one used here) for the deconvolution of maps (or linescans) is necessary to achieve correct datasets.

Further advices

If required three-dimensional insight into the specific IC internal block or its connection to nearby features (in a limited sub-volume) we can also suggest FIB 3D tomography or nano-CT analysis. However, both approaches require specially sample preparation, where site-specific sub-volume is carefully cropped out of a bulk IC component, and sub-volume sizes are limited in edge dimensions up to ~50 μm or ~200 μm for FIB3D or nano-CT technique, respectively.

This report has been written by Gregor Kapun and Mattia Fanetti (02/11/2021)